WHAT IS CLAIMED IS:

1. A memory controller having a first mode and a second mode, wherein said first mode has a memory access with the output of a column address and without the output of a row address, and said second mode has a memory access having precharge control after the output of a row address and a column address, the mode being switched to said first mode in the case of a memory access with the output of a row address and a column address following the precharge control in said first mode.

2. A memory controller according to claim 1, wherein the mode is switched to said first mode in response to an event of memory access with a same row address in said second mode.

3. A memory controller according to claim 2 further including a register for setting as to whether or not switching between said first mode and said second mode is to take place.

4. A memory controller according to claim 2, wherein said first mode is a page mode.

5. A memory controller according to claim 2, wherein said precharge control of said second mode is to put out a high-level RAS signal on expiration of a prescribed time length following the output of said column address.

6. A memory controller according to claim 2, wherein said precharge control of said second mode is to put out a precharge command on expiration of a prescribed time length following the output of said column address.

7. A data processing system comprising:

a central processing unit which puts out an address;

a memory controller which is supplied with the address and adapted to operate in a first mode or a second mode; and

a memory which is controlled by said memory controller,

wherein the mode of said memory controller is switched from said first mode to said second mode in response to an event of access to a first page of said memory and a subsequent event of access to a second page which is different from the first page in said first mode.

8. A data processing system according to claim 7, wherein the mode of said memory controller is switched from said second mode to said first mode in response to event of access to a third page of said memory and a subsequent event of access to the third page in said second mode.

9. A data processing system according to claim 8 further including a register circuit for setting as to whether or not switching between said first mode and said second mode is to take place.

10. A data processing system according to claim 9, wherein said central processing unit is capable of altering the setting of said register circuit.

11. A data processing system according to claim 8, wherein said central processing unit and said memory controller are formed on a same semiconductor chip.

12. A data processing system according to claim 8, wherein said central processing unit, said memory controller and said memory are formed in a same semiconductor package.

13. A memory controller comprising:

a plurality of input nodes where an address is inputted to;

a first register circuit which stores the address inputted to said input nodes;

a first comparator circuit comparing the address inputted to said input nodes with the address stored in said first register circuit;

a second comparator circuit comparing the contents of a second register circuit with the output of said first register circuit; and

a first circuit which is set in a first state or a second state depending on the output of said second comparator circuit.

14. A memory controller according to claim 13, wherein said first comparator circuit evaluates the number of times of comparison result indicative of the inequality between the address stored in said first register circuit and the address inputted to said input node, and said second comparator circuit compares the value provided by said first comparator circuit with the contents of said second register circuit.

15. A memory controller according to claim 13 further including:

a second circuit which outputs a first part and second part of the address inputted to said input node if said first circuit is set to said first state, or outputs the first part of the address inputted to said input node if said first circuit is set to said second state; and

an output node which outputs the output of said second circuit to a memory.

16. A memory controller according to claim 13, wherein said first register circuit stores part of the address inputted to said input node, and said first comparator circuit compares part of the address inputted to said input nodes with the part of the address stored in said first register circuit.

17. A memory controller according to claim 16, wherein said first comparator circuit compares a first address which is inputted to said input nodes with a second address which has been inputted to said input nodes in advance of the input of said first address to said input nodes.

18. A memory controller according to claim 13, wherein the address inputted to said input nodes has a plurality of bits, said first register circuit has a plurality of storing areas, and said first comparator circuit compares said first address with an address which is stored in one of said storing areas specified by a certain bit of said first address.

19. A memory controller according to claim 15, wherein said first part of the address is a row address of said memory, and

said second part of the address is a column address of said memory.

20. A memory controller according to claim 13, wherein said input nodes are supplied with an address outputted by a central processing unit.

21. A semiconductor device comprising: a memory controller receiving commands from a CPU, and controlling a memory including a plurality of memory banks, wherein said memory controller has a first mode and a second mode, wherein each of said plurality of memory banks comprises a plurality of word lines, data lines, and memory cells, wherein said memory is controlled to precharge after a read access in said first mode, wherein said memory is controlled to receive next access command without precharge operation after a read access in said second mode, wherein when a refresh command is received by said memory controller, said memory controller precharges said plurality of memory cells of said plurality of memory banks before refreshing said plurality of memory cells.

22. The semiconductor device according to claim 21, wherein a successive read access after refresh command is operated without a precharge operation.

23. The semiconductor device according to claim 22, wherein said memory controller comprises a page access decision circuit, a mode changing circuit, and an address generating circuit, wherein said page decision circuit compares a row address inputted to said memory controller

and the previous address, wherein said mode changing circuit receives signals from said page decision circuit and holds information of a number of consecutive access to each of said plurality of said memory banks, and wherein said address generating circuit receives signals from said page decision circuit and from said mode changing circuit and outputs bank active commands, bank addresses, row addresses, and column addresses to said memory.

24. The semiconductor device according to claim 23, wherein said memory controller further comprises a first and a second bus coupled to said address generating circuit, wherein said first bus is used for transferring commands and said second bus is used for transferring addresses.

25. The semiconductor device according to claim 23, wherein said memory is a SDRAM.

26. The semiconductor device according to claim 24, further comprising: a DRAM memory chip to be controlled by said memory controller, wherein said DRAM memory chip is molded in the same package as the memory controller.

27. The semiconductor device according to claim 24, wherein during said first mode if an access to a same word line continues, a precharge operation before a read operation is abridged, wherein during said second mode if an access to a different word line occurs, a precharge is operated before a read operation.